Remarks

Reconsideration of pending Claims 1-2, 4-23, 26-28, 30-34, 50-55, and 57-78 is respectfully requested.

Claims 1, 9, 11-13, 18, 22, 26-27, 32, 50, 58, 60-62, 64, and 69-76 have been amended. Claims 3, 24-25, 29, and 56 have been canceled. Claims 77-78 have been added.

Support for the amendments to the claims is in the claims as originally filed, the figures and throughout the specification. The amendments are intended to merely clarify language used in the claims, and the scope of the claims is intended to be the same as it was before the amendment in accordance with the invention. No new matter has been added with the amendments.

Rejections under 35 U.S.C. § 102(b)(e) (Preslar)

The Examiner rejected Claims 1, 2, 5, 7-14, 16-19, 21-24, 26-34, 50-53, 55, 57-65, and 69-76 as anticipated by USP 5,900,643 (Preslar). This rejection is respectfully traversed.

The Examiner cites Preslar as disclosing all of the elements of the claims. The Examiner particular cites to FIGS. 3-4 of Preslar.

As admitted by the Examiner (Office Action at page 20, paragraph 7), Preslar does not disclose a bond pad having a plurality of (at least two) lower metal layers with an overlying upper metal layer. Thus, Preslar does not teach or suggest Applicant's bond pad structure as recited in Claims 1, 9, 11-13, 18, 50, 58, 60-62, 69-70, 72-73, 75, or 77-78, nor the claims depending therefrom.

Also admitted by the Examiner (Office Action at page 20, paragraph 6), Preslar does not disclose first and second bond pads interconnected by a conductive solder material. Accordingly, Preslar does not teach or suggest Applicant's bond pad structure as recited in Claims 22, 71, or 77-78, nor the claims depending therefrom.

As for Claims 28, 32, 64, 74, 76, and 78, Preslar does not teach or suggest a bond pad structure comprised of first and second bond pads whereby a first bond pad is functional only in an operational mode, and a second bond pad is functional in a test mode and in an operation mode upon discontinuing the test mode and being interconnected to the first bond pad. Rather, Preslar teaches a bond pad structure whereby *both* bond pads function in a test mode and in an

operational mode. See Preslar at the Abstract, and at cols. 2-3 and cols. 3-4, bridging paragraphs (emphasis added):

> Abstract
>
> First and second electrical components on an integrated circuit chip are electrically connected respectively to a wire bonding pad and to a probe contacting area of a size significantly less than the bonding pad. The pad and contacting area are electrically isolated whereby both components *can be separately electrically tested by test probes contacting each of the pad and the contact area. After the components have been tested, the bonding pad and the probe contact area are electrically connected together for electrically connecting the first and second components.* ...
>
> .....
>
> SUMMARY OF THE INVENTION
>
> The invention resides, in part, in ...Thus, in contrast to the prior art structure described above, on chips embodying the invention *the separate testing of two components is made possible by* providing and connecting one bonding pad to one of the components, and providing and connecting a separate and smaller probe contacting "test" area electrically insulated from the bonding pad to the other of the two components. *Accordingly, both components can be separately and/or independently tested.* After the components have been tested, the test area and the bonding pad are electrically connected together directly on the chip, and only a single terminal wire is used for providing a common external connection for both components.
>
> .....
>
> DESCRIPTION OF A PREFERRED EMBODIMENT
>
> .....
>
> Because the composite pad portions 40 and 42 are electrically insulated from each other, separate electrical testing of the diode 20 and the transistor T16 is possible by means of separate test probes (not shown) *which are respectively brought into contact with the bonding pad large portion 40 and the test pad 46*.
>
> After testing, the chip is mounted in a package, not shown, and terminal wires are bonded to each of the bonding pads 30 and 36, but not to the test pad 46....

By comparison, Applicant is claiming a bond structure in the form of two separate bond pads — one functional in a test mode and an operational mode, and the other functional only in an operational mode. This is described, for example, in the specification at page 1 at lines 19-26, at page 4, lines 3-9, and at page 9, lines 13-25, as follows (emphasis added):

> BACKGROUND OF THE INVENTION
>
> ...
>
> In some constructions, the test bond pad is not disabled but is converted to an operational mode. However, in shorting a fuse or using a high voltage to disable a transistor to terminate the test mode, leakage problems can result. The separation of the test mode from the operational mode would help solve this problem. The separation would also protect operational devices from high voltages during testing. It would be desirable to provide such a structure in the form of two separate bond pads, *one bond pad functional in a test mode and, when connected to the other bond pad, both functioning as a single pad in a operational mode*. In fabricating such a bond pad structure, consideration must be given to the structuring of the two bond pads in conjunction with each other.

...

SUMMARY OF THE INVENTION

...

In yet another aspect of the invention, a method of testing and/or operating an integrated circuit using an integrated circuit die comprising a bond pad structure as described herein, is provided. An embodiment of a bond pad structure of an integrated circuit die for use in testing and operating circuitry, comprises *a first bond pad which is a test mode bond pad* that receives and responds to a test mode signal and, after the test sequence is complete and the first and a second bond pad of the bond pad structure are interconnected with a conductive material, the first and second bond pads function as a single unit to receive and respond to any signal.

...

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

...

In an exemplary bond pad structure according to the invention for use in testing and operating circuitry, *the first bond pad 28' can comprise an operational mode bond pad that functions in an operational mode. The second bond pad 30' can comprise a test mode bond pad that functions initially in a test mode for testing of circuitry and subsequently, upon completion of the circuit testing and its connection to the first bond pad 28', in an operational mode as a single unit with the first bond pad 28'.* The connection between the first and second bond pads 28', 30' can be performed by applying a conductive material 44' (e.g., solder) over at least a portion of each of the bond pads 28', 30' to form an extension between the two pads. It is understood that the first bond pad can be a test mode bond pad and the second bond pad can be an operational mode bond pad. Such a structure is useful for testing an integrated circuit, and functioning in an operational mode once the individual bond pads are connected. The separation of the first and the second bond pads 28', 30' avoids leakage problems that can be caused by high voltage that is applied when the fuse or antifuse is blown at the end of a test operation.

Preslar does not teach or suggest a bond pad structure as recited in any of Claims 1, 2, 5, 7-14, 16-19, 21-24, 26-34, 50-53, 55, 57-65, and 69-76. Accordingly, withdrawal of the rejection of the claims based on Preslar is respectfully requested.

Rejections under 35 U.S.C. § 102(e) (Muramatsu)

The Examiner rejected Claims 1-4 and 9 as anticipated by USP 6,420,664 (Muramatsu). This rejection is respectfully traversed.

The Examiner cites Muramatsu as disclosing all of the elements of the claims. The Examiner particular cites to FIGS. 1 and 18 of Muramatsu, and a purported "bond pad structure (26)."

Fig.1

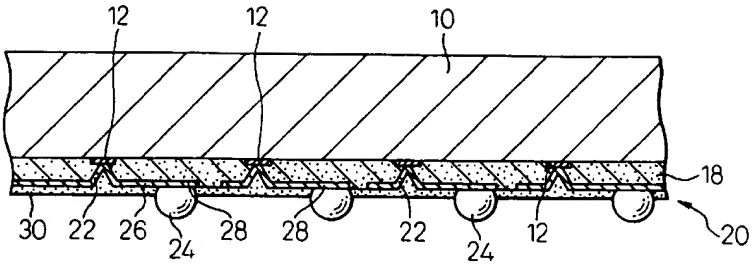

FIG. 1 illustrates a semiconductor die 10 having "electrode terminals" 12 disposed on a surface, with the die 10 being mounted on a sheet of metal foil 20.

FIG. 1 is described at col. 6, lines 1-19, as follows:

> Semiconductor Device
>
> FIGS. 1 to 3 are cross-sectional views respectively showing an arrangement of the semiconductor device manufactured by using a sheet of metal foil 20 having bumps.
>
> FIG. 1 is a cross-sectional view showing a semiconductor device manufactured in such a manner that *the sheet of metal foil 20 having bumps is made to adhere onto an electrode terminal carrying surface of the semiconductor chip 10 via the adhesive agent layer 18*. This sheet of metal foil 20 having bumps used for the semiconductor device is composed in such a manner that the bumps 22 are formed on the sheet of metal foil in the same plane arrangement as that of the electrode terminals 12 formed on the electrode terminal carrying surface. As shown in the drawings, the sheet of metal foil 20 having bumps *is made to adhere onto* the electrode terminal carrying surface of the semiconductor chip 10 via the adhesive agent layer 18 under the condition that each forward end portion of the bump 22 comes into contact with each electrode terminal 12.

First of all, the metal foil layer 20 is *adhered to* the surface of the die (10).

Secondly, element 26 is *not* a bond pad structure. Rather, element 26 is a wiring pattern within substrate 20, which functions to electrically connect "bumps" 22 to external ball connections 24.

Fig.18

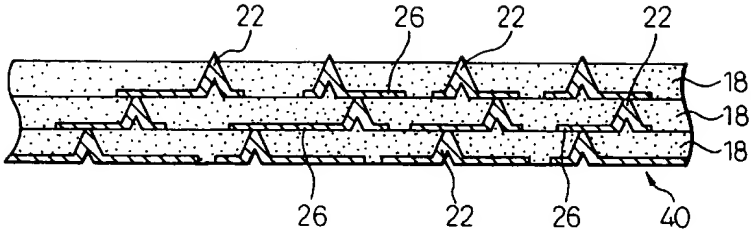

FIG. 18 is an illustration of a multi-layer circuit substrate 40, which is described at col. 14, lines 17-29 (emphasis added):

> Multilayer Circuit Substrate
>
> All of the aforementioned circuit substrates are composed of a single layer. However, it is possible to provide a *multilayer circuit substrate* by laminating circuit substrates 40 on which the adhesive agent layers 18 are provided on the faces on which the bumps 22 are formed.
>
> *FIG. 18 is a view showing an embodiment of the multilayer circuit substrate*. The circuit substrates 40 having the same *wiring patterns 26* as those of the circuit substrate shown in FIG. 17 are laminated and adhere to each other by the adhesive agent layers 18, so that the multilayer circuit substrate can be obtained.

The multi-layer circuit structure 40 illustrated by FIG. 18 is *not* bond pads of a semiconductor die.

FIGS. 19(a1) to 19(c) illustrate Muramatsu's method of manufacturing a semiconductor device, which is described at col. 15, lines 7-16 (emphasis added):

> Method of Manufacturing Semiconductor Devices
>
> ...
>
> FIGS. 19(a1) to 19(c) are views showing a method by which the semiconductor device 50 is formed *by making the circuit substrate 40 adhere to the semiconductor chip 10*. The semiconductor chip 10 and the circuit substrate 40 are positioned with each other as shown in FIGS. 19(a1) and 19(a2), and *the circuit substrate 40 is made to adhere to the semiconductor chip 10* as shown in FIG. 19(b). Then, the external connection terminals 24 such as solder balls are joined to the lands 28. In this way, the semiconductor device 50 can be made as shown in FIG. 19(c).

Fig.19(a1)

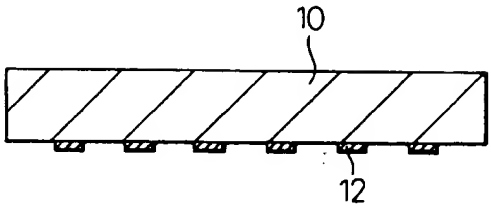

Figure 19(a1) illustrates electrode terminals 12 on a semiconductor chip 10.

Fig.19(c)

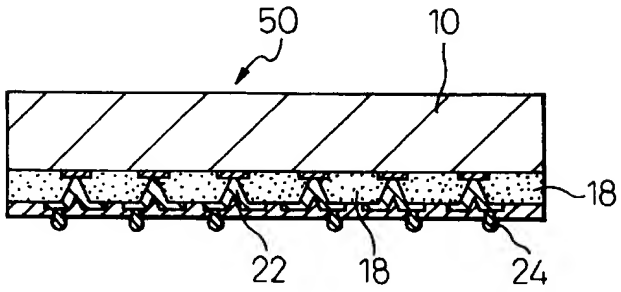

FIG. 19(c) illustrates the chip 10 adhered to a circuit substrate 40.

Neither wiring element 26 nor circuit substrate 40 are structurally or functionally the same as a bond pad structure. Circuit substrate 40 (with wiring element 26):

-- is *not* part of a bond pad structure;

-- is a separate element that is adhered onto terminals 12 on the die surface; and

-- functions as a substrate for mounting a die or chip (10) onto an external element via external connection terminals 24 (i.e., solder balls).

Clearly, circuit substrate 40 (and wiring element 26) is not part of a bond pad structure.

The Examiner has mischaracterized the meaning of a "bond pad" as that structure is understood in the art.

The Examiner is again respectfully directed to Wolf and Tauber, *Silicon Processing for the VLSI Era* (vol. 1), Lattice Press, Sunset Beach, CA (2000) at pages 827-829, which describes

bonding pads as metal patterns *exposed on a chip through openings* etched into a passivation layer deposited onto a wafer surface.[1]

> **16.2.12 Passivation Layer and Pad Mask**: Finally, a *passivation* (or *overcoat*) layer...is put down onto the wafer surface...
>
> Openings are etched into this layer so that a set of special metallization patterns under the passivation layer is exposed. These metal patterns are normally located in the periphery of the circuit and are called *bonding pads* (FIG. 16-20)...Wires are connected (bonded) to the metal of the bonding pads and then bonded to the chip package...

Maramatsu provides no discussion on the formation of bond pads.

Neither element 26 nor multilayer circuit substrate 40 in Maramatsu functions or is structurally the same as a bond pad structure. Accordingly, withdrawal of this rejection is respectfully requested.

Rejection under 35 U.S.C. §103(a) (Preslar with Geffken)

The Examiner rejected Claims 6, 15, 20, 25 and 54 under Section 103(a) as obvious over Preslar in view of USP 5,883,435 (Geffken). This rejection is respectfully traversed.

The Examiner maintains, although Preslar does not disclose the use of a conductive material comprising a solder material or solder, it would be obvious to utilize such material to connect the two bond pads, based on the disclosure in Geffken "for at least the purpose of increasing the bond strength between the pads and the external device (e.g., wire)" (Office Action at page 20, paragraph 6).

Geffken does not teach or suggest employing a solder to interconnect bond pads of a semiconductor device. Geffken teaches depositing solder bumps onto a *transition layers* 160, 162, 164. The transition layers (e.g., Cr/Cu/Au sandwich) are formed over contacts as a *barrier layer* to *isolate* the bump array material from the underlying metal layer. This is described at col. 4, line 59 to col. 5, line 18 (emphasis added):

> Turning now to FIG. 6, the next step is to deposit a conductive transition layer over each contact. In the illustrated example *transition layers 160, 162 and 164 are deposited over the*

---

[1] See also, Stanley Wolf, *Silicon Processing for the VLSI Era* (vol. 2), Lattice Press, Sunset Beach, CA (1990) at page 377. See also Peter Van Zant, *Microchip Fabrication*, 4th ed., McGraw-Hill, New York, NY (2000): at pages 82-83 illustrating bonding pads (3) on a chip; at page 560: "...the chip wiring terminates in the larger bonding pads around the edge of the chip;" and the definition of "bonding pads" at page 596:

> **bonding pads** Electrical terminals on the chip (generally around the periphery) used for connection to the package electrical system.

various contacts. The transition layer serves as a mechanically strong bonding layer to semiconductor device. In particular the transition layer prevents the bumps in the array from moving horizontally as they are heated. *The transition layer also serves as a barrier layer to keep the bump array material from reacting with the underlying metallurgy.* For example, the preferred transition layer comprises a sandwich of chrome, copper and gold with a transition phase of chrome/copper between the chrome and copper. Of course, other suitable materials can be used such as TiCuAu or TiNiCuAu.

...

Turning now to FIG. 7, the next step is to deposit a bump array on the semiconductor device, *with a bump deposited on each transition layer*. In the illustrated embodiment a bump 170, 172 and 174 is deposited on transition layers 160, 162 and 164 respectively....

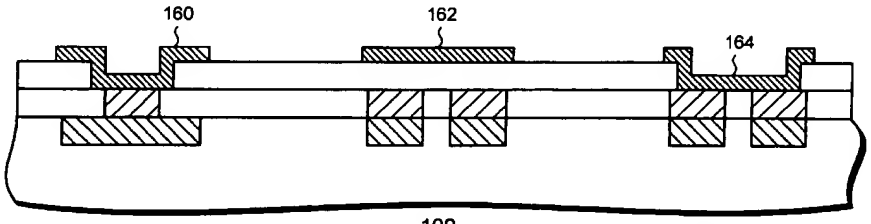

FIG. 6

FIG. 6 illustrates conductive transition layers 160, 162 and 164 deposited over the various contacts.

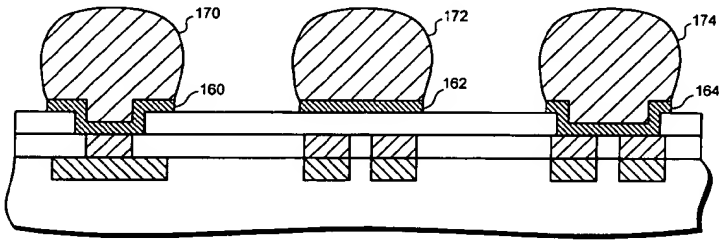

FIG. 7

FIG. 7 illustrates embodiment a bump 170, 172 and 174 deposited on transition layers 160, 162 and 164 respectively.

Geffken does not teach or suggest employing a solder to interconnect bond pads of a semiconductor device.

There is no motivation in either Preslar nor Geffken to utilize a solder material to connect bond pads in a semiconductor construction. Accordingly, withdrawal of this rejection of the claims is respectfully requested.

Rejection under 35 U.S.C. §103(a) (Preslar with Muramatsu)

The Examiner rejected Claim 56 under Section 103(a) as obvious over Preslar in view of Muramatsu. This rejection is respectfully traversed.

The Examiner admits that Preslar does not disclose a plurality of lower metal layers in a bond pad structure, but cites Muramatsu as motivation to alter Preslar to incorporate a plurality of lower metal layers.

As previously stated, Maramatsu does not teach element (26) as part of a bond pad structure. Rather, element (26) is wiring in a *multilayer circuit substrate* (40), which is adhered onto terminal (12) of die (10) for mounting the die via solder balls (24) onto an external substrate. Maramatsu provides no information on the formation of bond pads.

Neither element (26) nor substrate 40 in Maramatsu functions or is structurally the same as a bond pad structure.

Thus, the combination Preslar with the disclosure of Muramatsu would not provide Applicant's bond pad structure as claimed. Accordingly, withdrawal of this rejection is respectfully requested.

In sum, neither Preslar nor Muramatsu, either alone or combined together or with the secondary reference of Geffken, teach or suggest Applicant's bond pad structure as claimed. Accordingly, withdrawal of these rejections is respectfully requested.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

Excess fees for added claims. Two claims (77-78) have been added. If any fees are required, please charge to Account No. 23-2053.

Based on the above remarks, the Examiner is again respectfully requested to reconsider and withdraw the rejections of the claims.

Respectfully submitted,

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Dated: April 16, 2004

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